AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Original) An apparatus for recovering the clock from an input serial data stream, comprising:

an N bit sequence shift register adapted to receive said serial data;

a comparator adapted to compare an upper half of said sequence shift register against a lower half thereof to produce a comparison result;

an integrator adapted to integrate said input serial data stream to produce an integrator result;

a correction circuit operative to generate a timing correction comprising direction and gain portions thereof based on said comparison result and said integrator result during a learning cycle; and

a clock generator circuit adapted to generate a recovered clock signal and to either retard, advance or not change the timing of said recovered clock signal in accordance with said timing correction during a correction cycle.

2. (Original) The apparatus according to claim 1, wherein said clock generator circuit applies said timing correction by adding or removing zero or more clock periods to or from said correction cycle whose initial or nominal length is N clock periods.

3. (Original) The apparatus according to claim 1, wherein said clock generator circuit is adapted to generate a clock transition between the N/2 and N/2-1 clock periods during said learning cycle.

4. (Original) The apparatus according to claim 1, wherein said clock generator circuit is adapted to generate a clock transition between the N/2 and N/2-1 clock periods during said correction cycle.

5. (Currently amended) The apparatus according to claim 1, wherein said ~~value of~~ N ~~comprises the~~ is a number the result of a ratio between an oversampling rate and the receive data bit rate.

6. (Currently amended) The apparatus according to claim 1, wherein said upper half of said sequence shift register comprises ~~the~~ most significant N/2 bits thereof wherein N is a number the result of a ratio between an oversampling rate and the receive data bit rate.

7. (Currently amended) The apparatus according to claim 1, wherein said lower half of said sequence shift register comprises ~~the~~ least significant N/2 bits thereof wherein N is a number the result of a ratio between an oversampling rate and the receive data bit rate.

8. (Original) The apparatus according to claim 1, wherein said clock generator comprises a reference counter operative to preload said timing correction at the start of each said correction cycle and to preload a fixed value of N-1 during learning cycles.

9. (Original) The apparatus according to claim 1, wherein said correction circuit comprises a direction look up table (LUT) adapted to generate said timing correction comprising left, right or no change signals in accordance with the sign of said integrator result and said comparator result.

10. (Original) The apparatus according to claim 1, wherein said correction circuit comprises a gain look up table (LUT) adapted to generate said timing correction comprising a gain signal in accordance with the magnitude of said integrator result.

11. (Original) The apparatus according to claim 1, wherein said correction circuit comprises:

a direction circuit adapted to generate 'left', 'right' or 'no change' signals in accordance with the sign of said integrator result and said comparator result;

a gain circuit adapted to generate a gain signal in accordance with the magnitude of said integrator result; and

a data load circuit adapted to generate said timing correction as a function of said 'left', 'right', 'no change' and gain signals.

12. (Original) The apparatus according to claim 1, wherein said clock generator comprises a counter adapted to be preloaded with a value of N-1 plus said gain to retard the timing of said recovered clock signal.

13. (Original) The apparatus according to claim 1, wherein said clock generator comprises a counter adapted to be preloaded with a value of N-1 minus said gain to advance the timing of said recovered clock signal.

14. (Original) An apparatus for recovering the clock from an input serial data stream, comprising:

means for initiating learning cycles during which a timing correction is generated and to initiate correction cycles during which said timing correction is applied to a recovered clock signal;

an N bit sequence shift register adapted to receive said serial data;

a comparator adapted to compare an upper half of said sequence shift register against a lower half thereof to produce a direction signal therefrom;

an integrator adapted to integrate said input serial data stream to produce a gain signal, said integrator adapted to be reset at the start of each learning cycle;

a correction circuit operative to produce during learning cycles direction and gain corrections base don said direction signal and said gain signal; and

a clock generator circuit adapted to generate said recovered clock and to adjust during correction cycles the timing of said recovered clock in accordance with said direction and gain corrections.

15. (Original) The apparatus according to claim 14, wherein said clock generator circuit comprises a counter adapted to be preloaded with a value of N-1 plus said gain correction to retard the timing of said recovered clock signal.

16. (Original) The apparatus according to claim 14, wherein said clock generator circuit comprises a counter adapted to be preloaded with a value of N-1 minus said gain correction to advance the timing of said recovered clock signal.

17. (Original) An apparatus for recovering the clock from an input serial data stream, comprising:

an N bit sequence shift register adapted to receive said serial data;

comparator means for comparing an upper half of said sequence shift register against a lower half thereof to produce a direction signal;

an integrator adapted to integrate said input serial data stream to produce a gain signal;

correction means for generating during a learning cycle a direction correction and a gain correction based on said direction signal and gain signal; and

a clock generator circuit adapted to generate a recovered clock signal whose timing is adjusted in accordance with said direction correction and gain correction during a correction cycle adapted to follow said learning cycle.

18. (Original) The apparatus according to claim 17, wherein said clock generator circuit is adapted to either retard, advance or not change the timing of said recovered clock signal in accordance with said direction correction.

19. (Original) The apparatus according to claim 17, wherein said clock generator circuit comprises a counter adapted to be preloaded with a value of N-1 plus said gain correction to retard the timing of said recovered clock signal.

20. (Original) The apparatus according to claim 17, wherein said clock generator circuit comprises a counter adapted to be preloaded with a value of N-1 minus said gain correction to advance the timing of said recovered clock signal.

21. (Original) The apparatus according to claim 17, wherein said clock generator circuit is adapted such that said direction correction determines whether said recovered clock signal is to be retarded, advanced or not changed while the degree of any retarding or advancing of the timing is determined by said gain correction.

22. (Original) A method of recovering a clock from an input serial data stream, said method comprising the steps of:

initiating learning cycles during which a timing correction is generated and initiating correction cycles during which said timing correction is applied to a recovered clock signal;

loading said serial data into an N bit sequence shift register;

comparing an upper half of said sequence shift register against a lower half thereof so as to produce a directions signal therefrom;

integrating said serial data stream so as to produce a gain signal;

generating during learning cycles said timing correction comprising direction and gain corrections based on said direction signal and said gain signal; and

generating said recovered clock signal whereby the timing of said recovered clock is adjusted in accordance with said direction and gain corrections during correction cycles.